

100 →

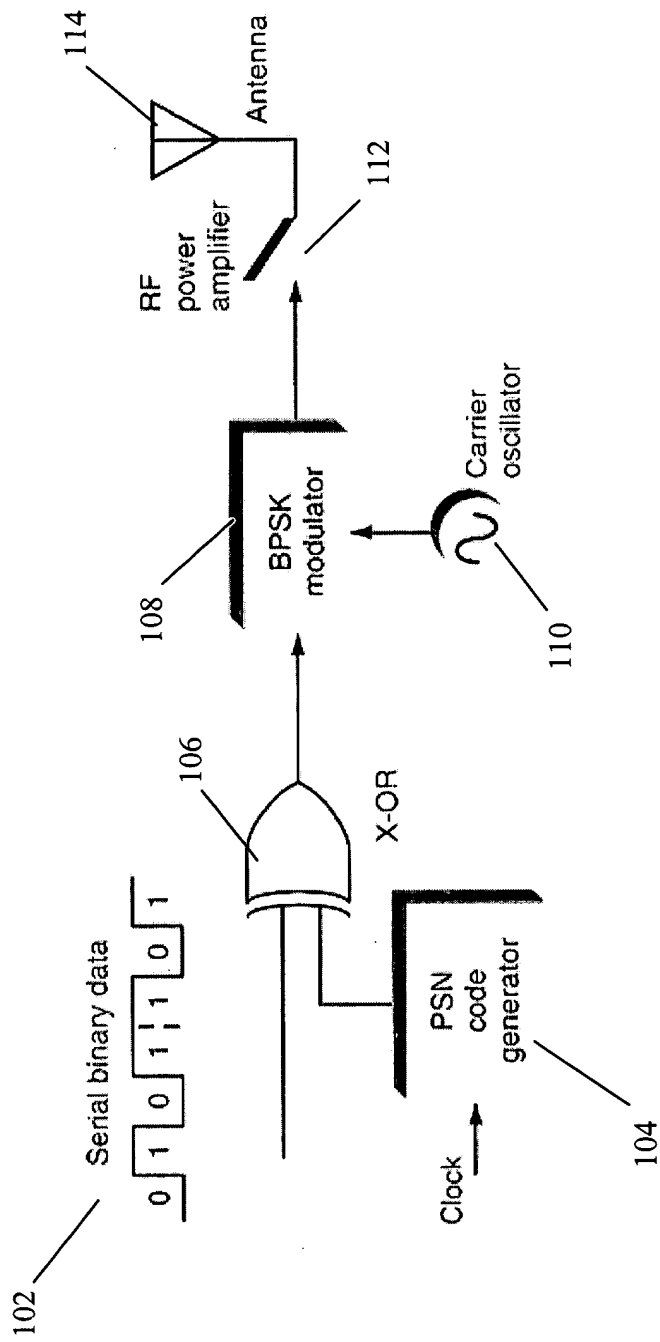


FIG. 1

(PRIOR ART)

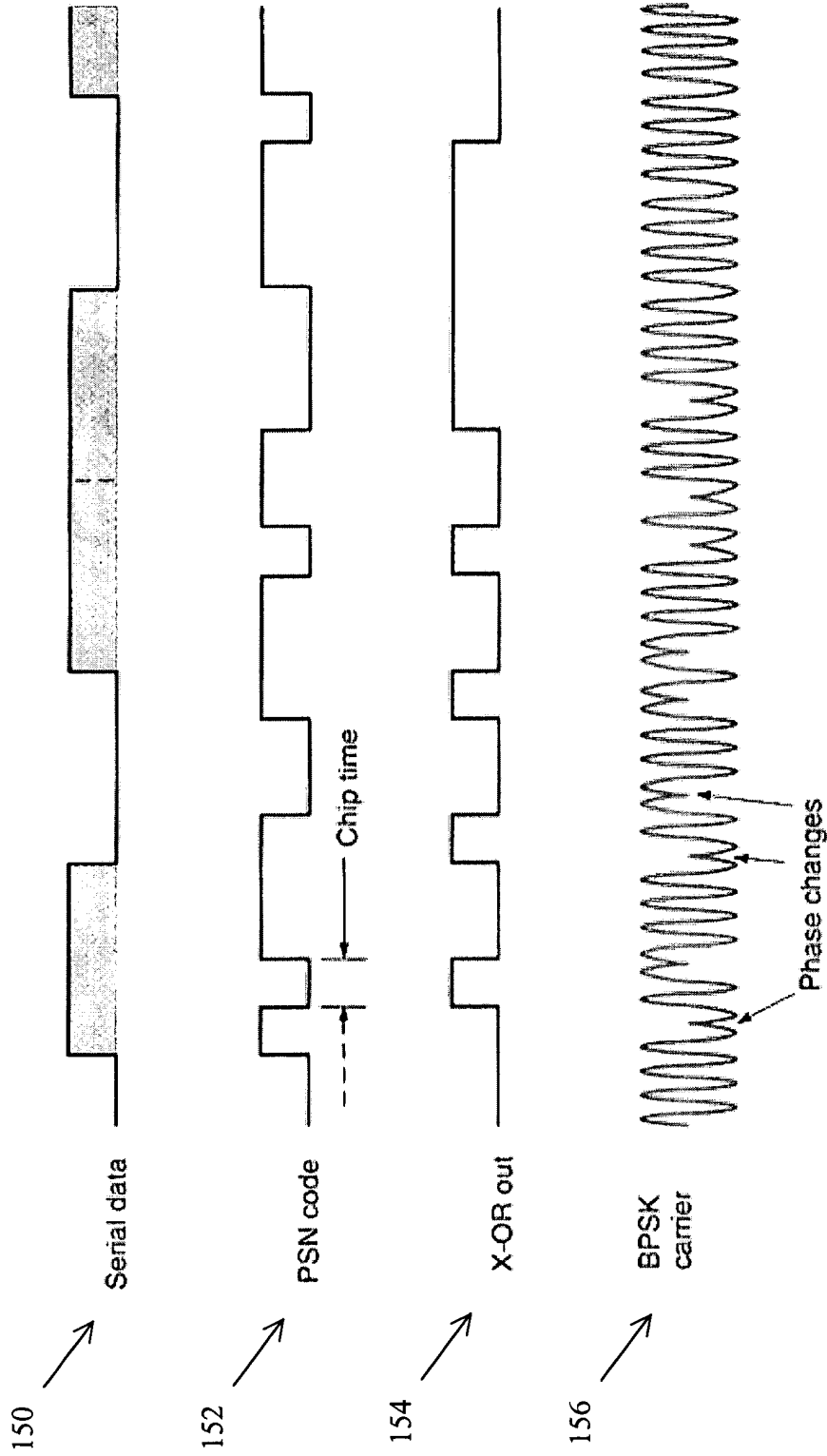


FIG. 2
(PRIOR ART)

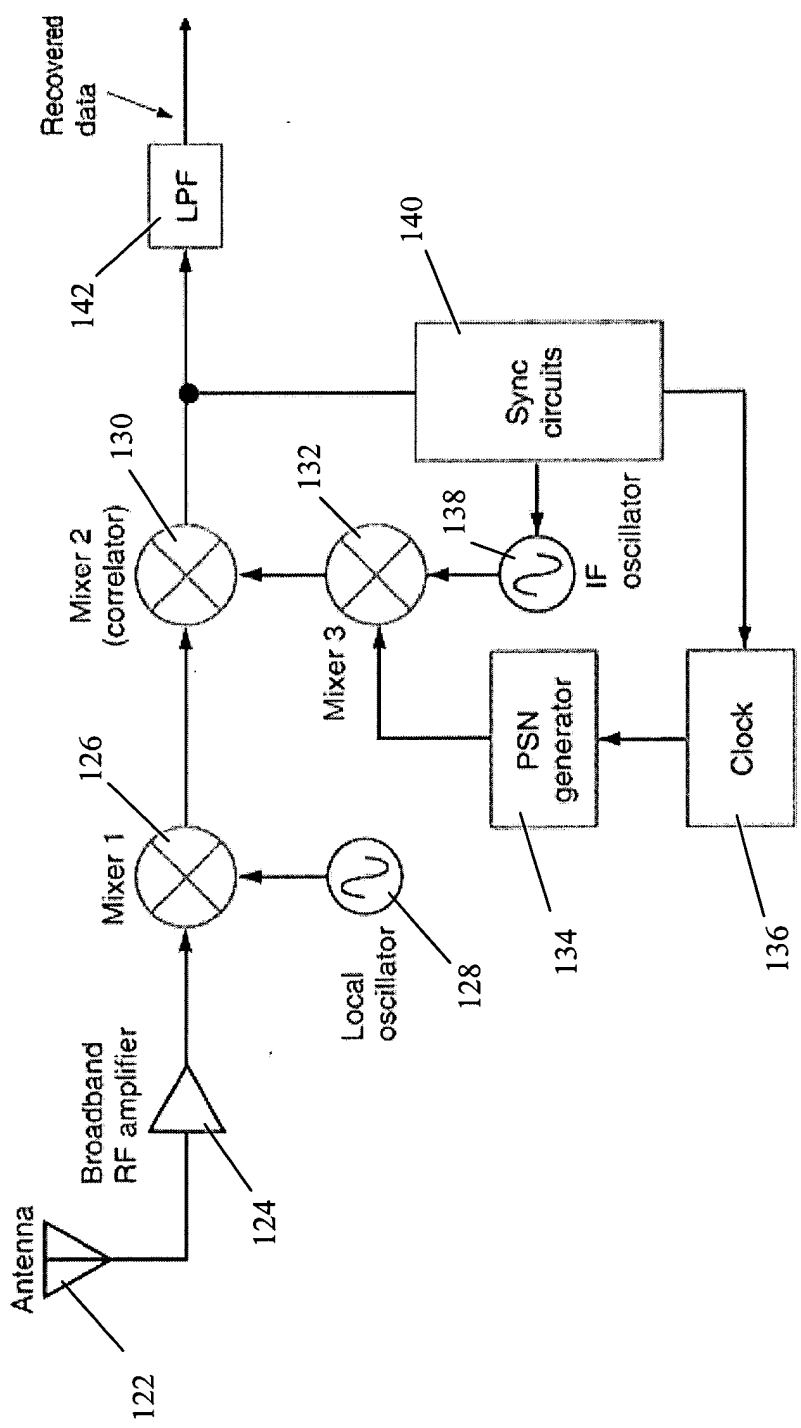


FIG. 3
(PRIOR ART)

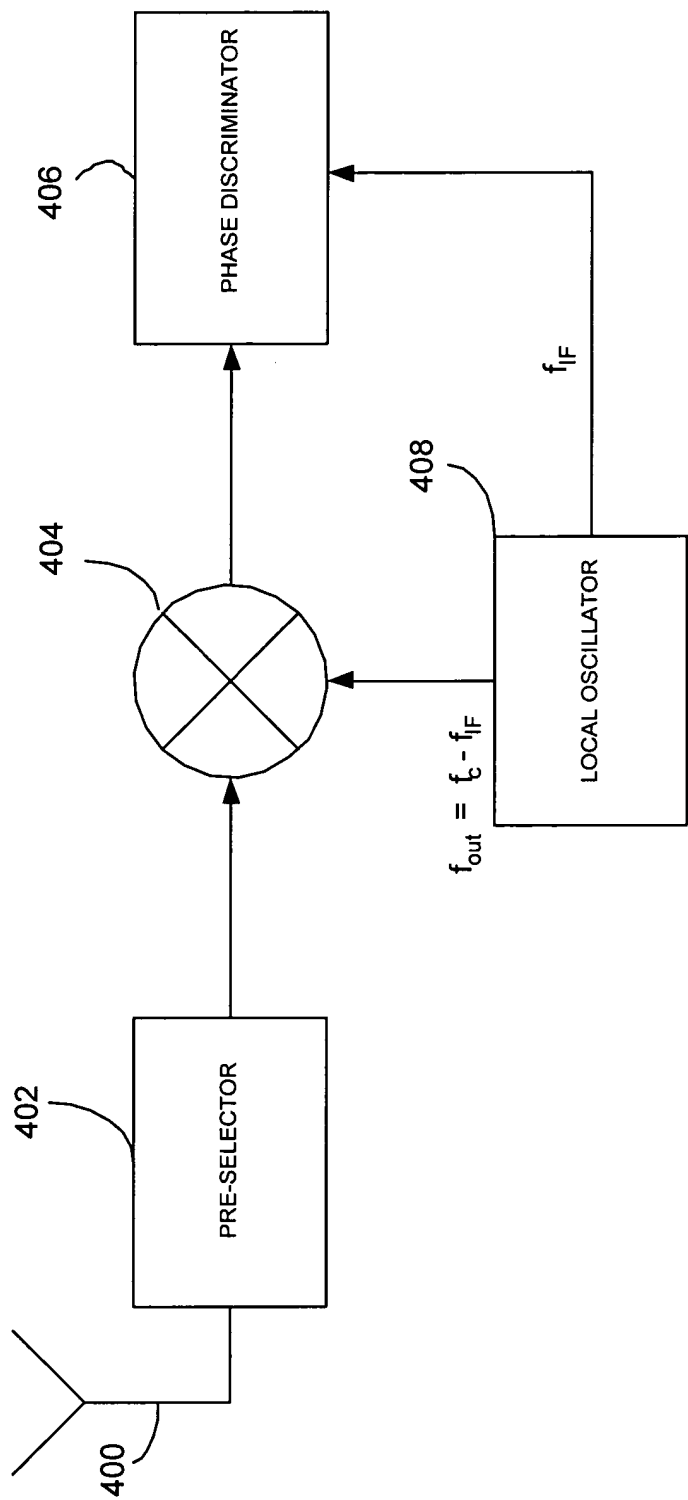


FIG. 4
(PRIOR ART)

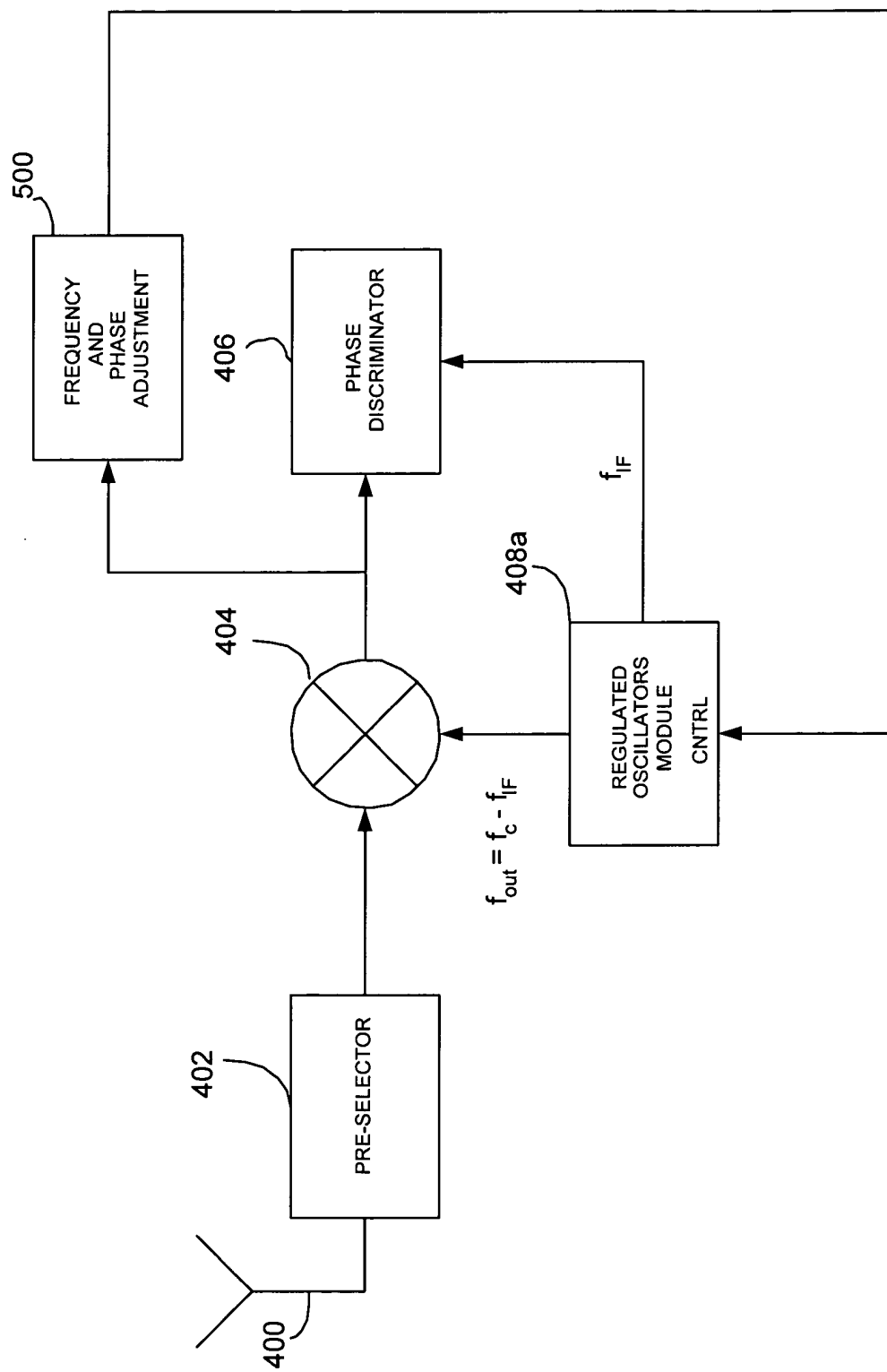


FIG. 5
(PRIOR ART)

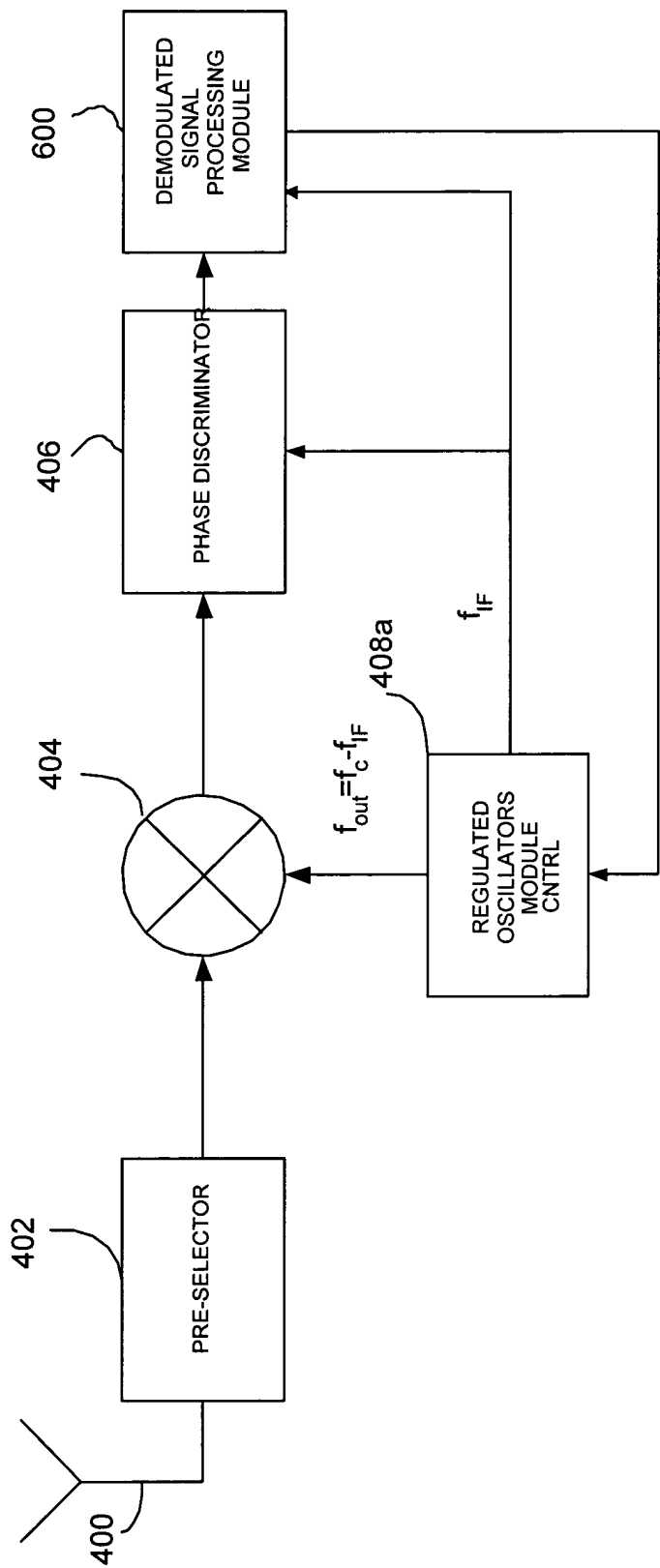


FIG. 6
(PRIOR ART)

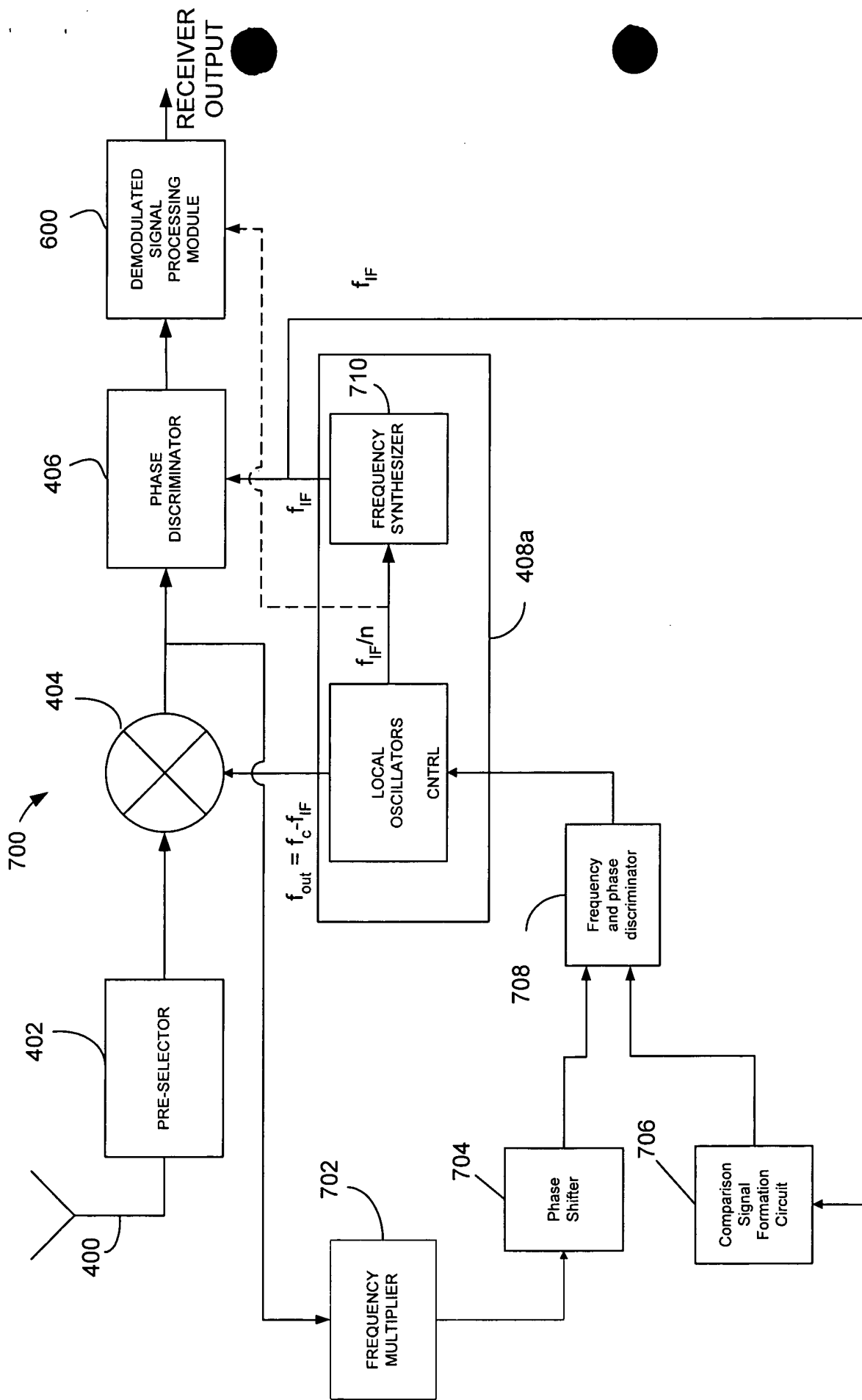


FIG. 7

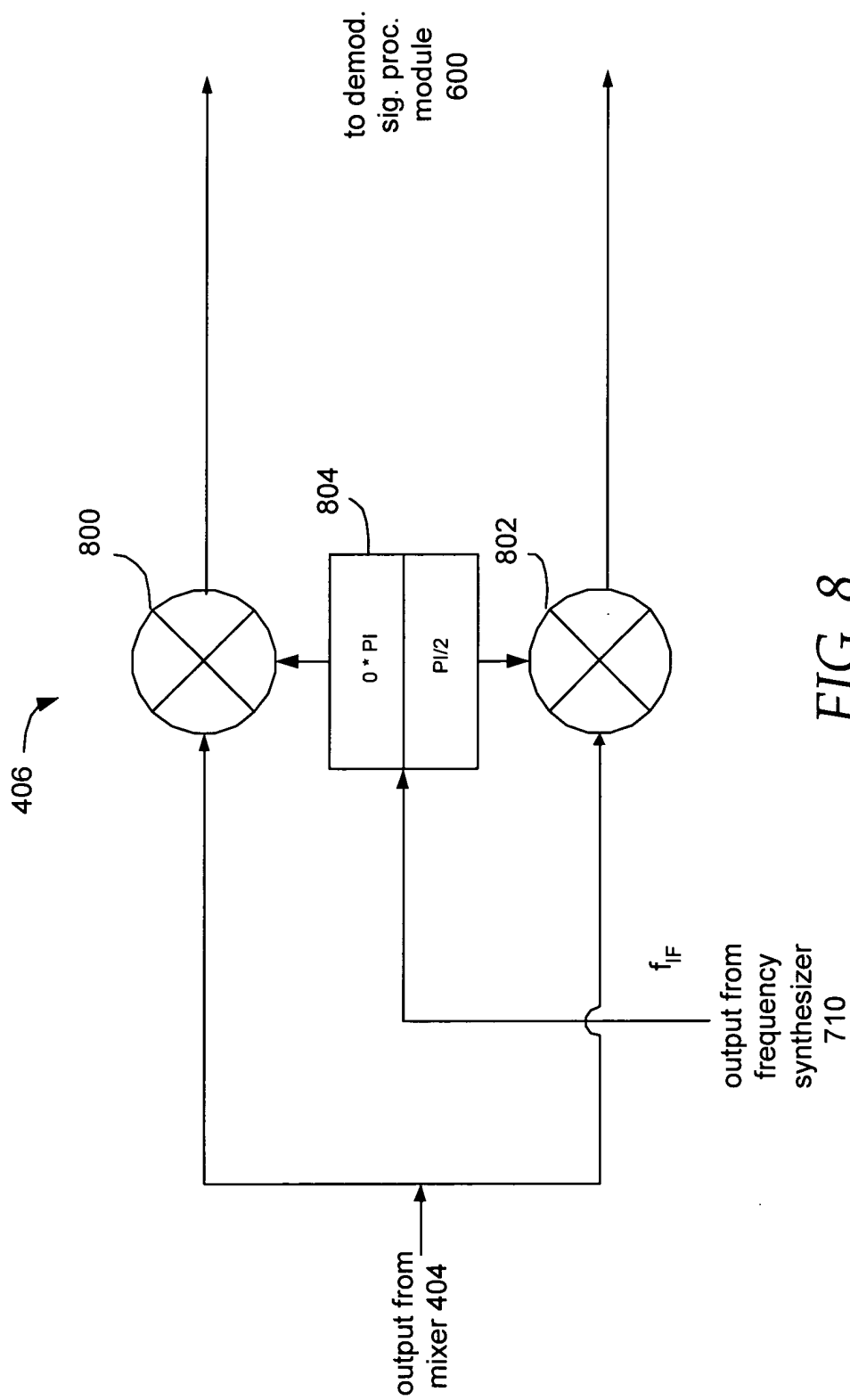


FIG. 8

702

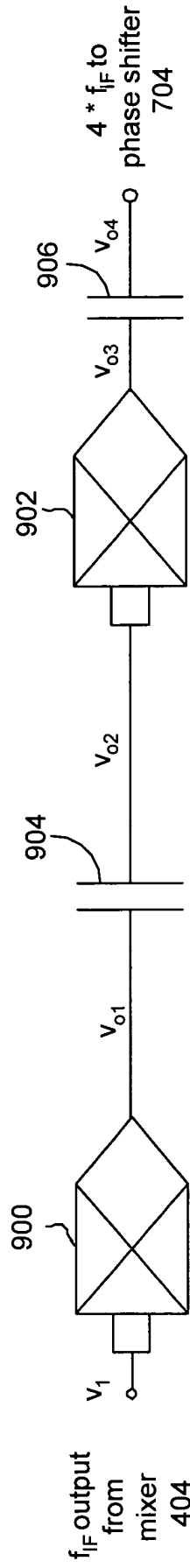


FIG. 9

FIG. 10 is a schematic diagram of a circuit for a frequency multiplier and phase discriminator.

704

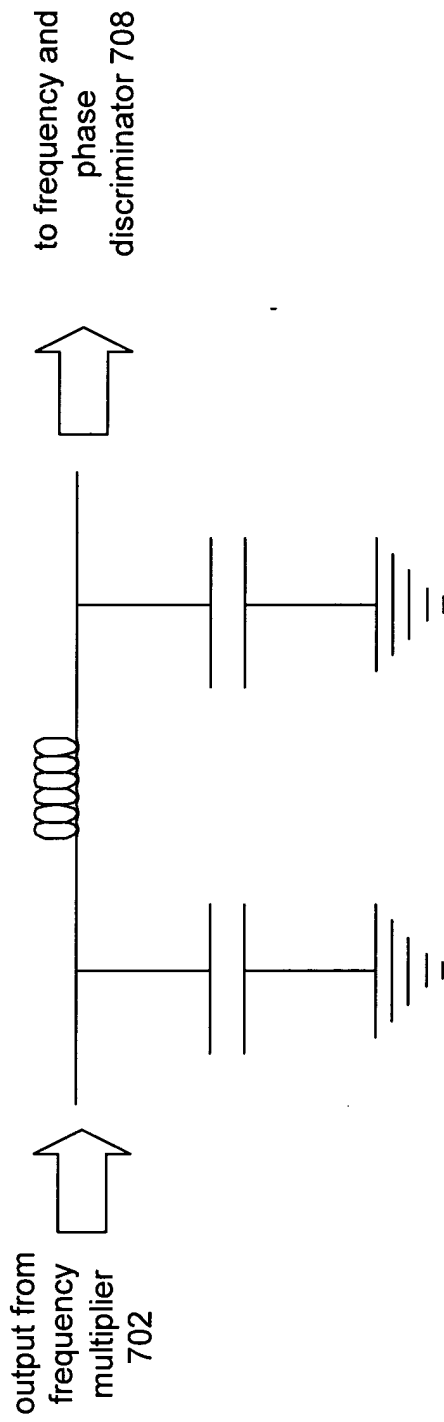


FIG. 10

706

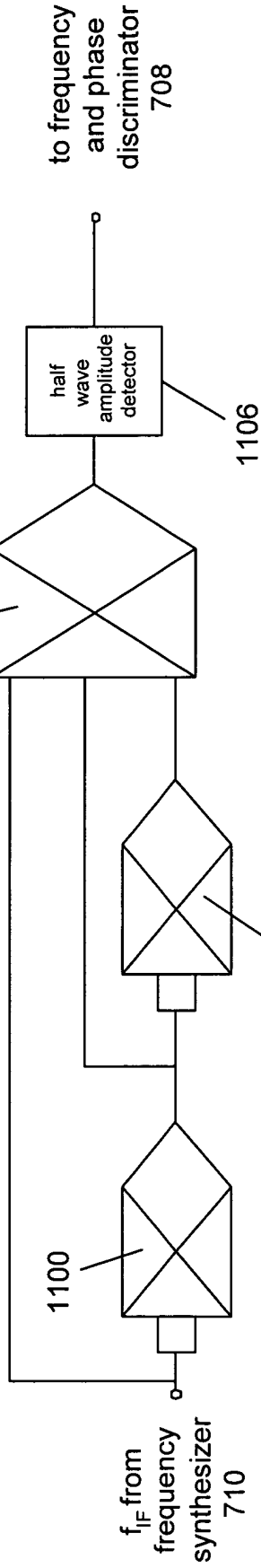


FIG. 11

FIG. 12

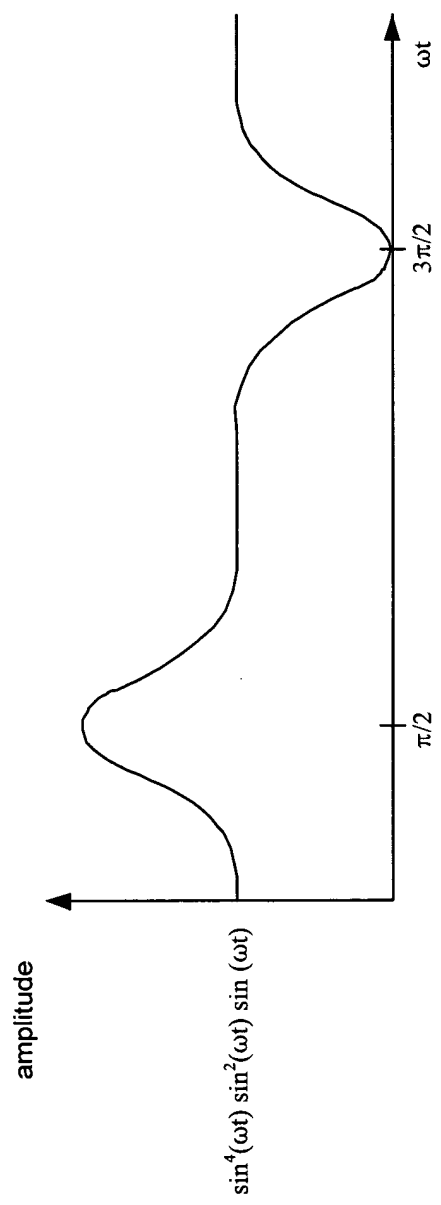


FIG. 12

FIG. 13 is a schematic diagram of a phase-locked loop (PLL) circuit, showing a phase shifter 704, a phase detector 706, a voltage-controlled oscillator (VCO) 1402, and a feedback loop 708.

708

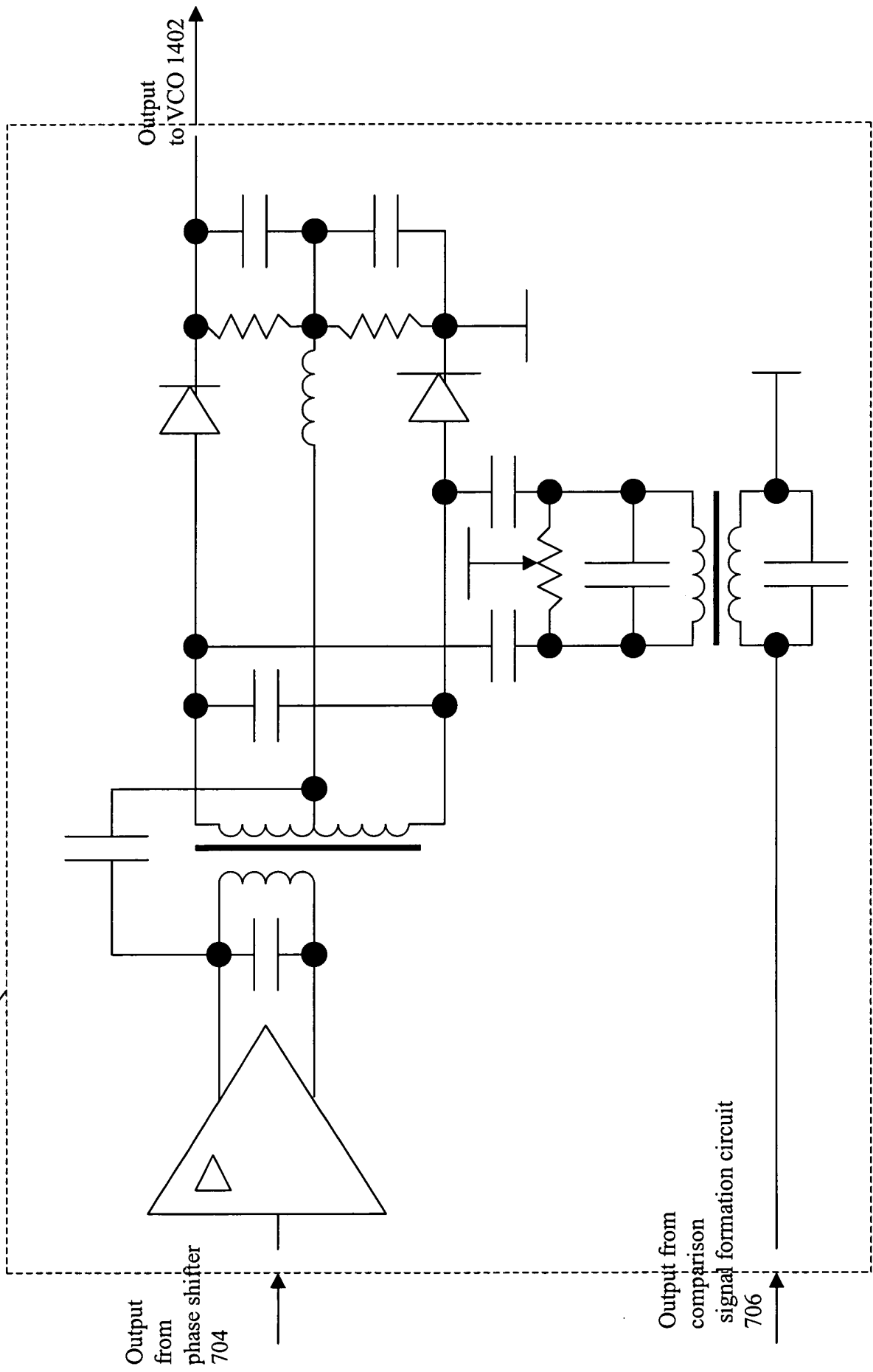


FIG. 13

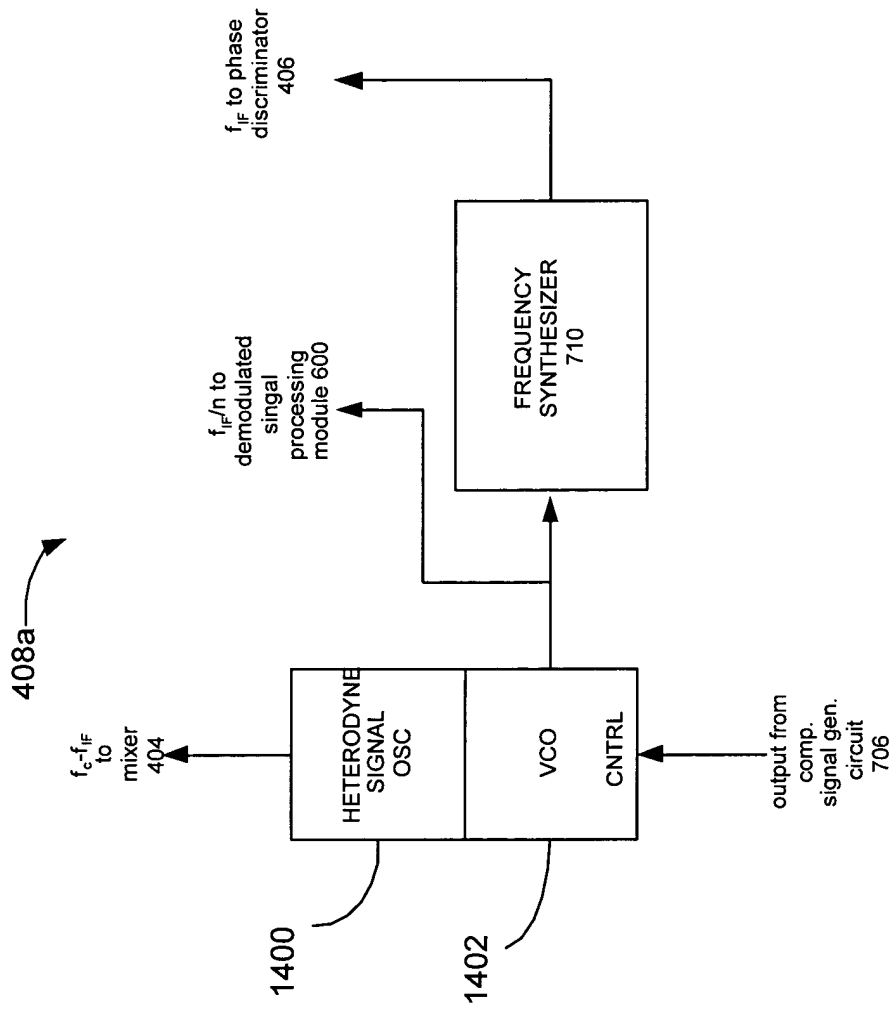


FIG. 14